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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

John W. ANDREWS et al.

Serial No.: 09/883,981 Group Art Unit: 2813

Filed: June 20, 2001 Examiner: David S. Blum

For: LOW COST SHALLOW TRENCH ISOLATION USING NON-CONFORMAL DIELECTRIC MATERIAL

Honorable Commissioner of Patents
Washington, D.C. 20231
Box AF

OK to enter with RCE 7/17/03 PSM

AMENDMENT UNDER 37 C.F.R. §1.116

Sir:

In response to the Final Office Action dated December 30, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

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SUB G1 F1

8. (Four Times Amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of seamless HDP oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

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15. (Five Times Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said

unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants, and

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

23. (Five Times Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants, and

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

24. (Amended) The semiconductor substrate according to claim 8, wherein said density plasma oxide comprises non-conformal high density plasma oxide.

26. (Amended) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises a dopant.

27. (Amended) The semiconductor substrate according to claim 1, wherein said high density plasma oxide comprises silicon dioxide.

31. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of seamless HDP oxide and said upper surface of said non-trench region are planarized without chemical mechanical polishing.

F6 cont. Sub G1

32. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of ~~said~~ single layer of seamless HDP oxide is substantially scratch-free.

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35. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of seamless HDP oxide is free of chatter marks.

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